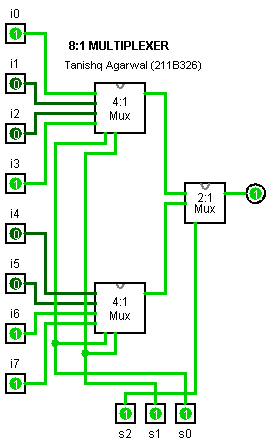
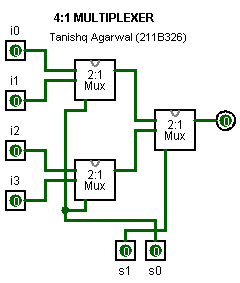
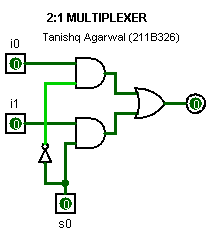
**EXPERIMENT#3**

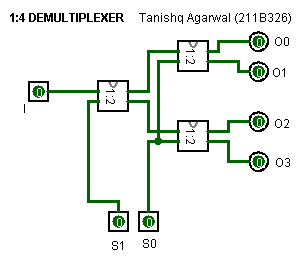
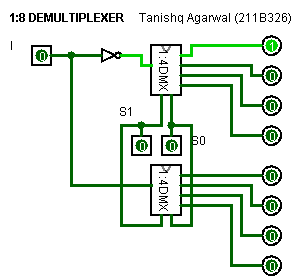
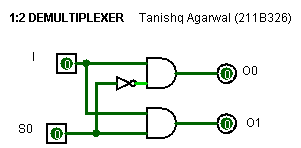
**Aim: Design of basic combinational logic circuits. (MUX, DEMUX,ENCODER, DECODER)**

**Exercise#1:** Design an 8:1 multiplexer using two 4:1 multiplexers and one 2:1 multiplexer (shown in Fig.1) Use both types of multiplexers as sub circuits in the design.

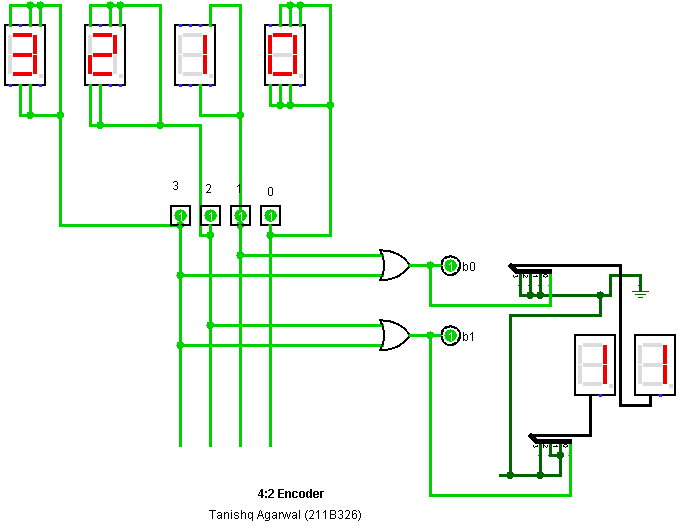
**Logic Diagram & SubCircuits:**

**Exercise#2:** Design a 1:8 de-multiplexer using three 1:4 de-multiplexers. Use 1:4 de-multiplexers as sub circuits in the design.

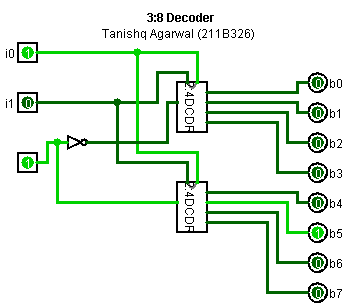
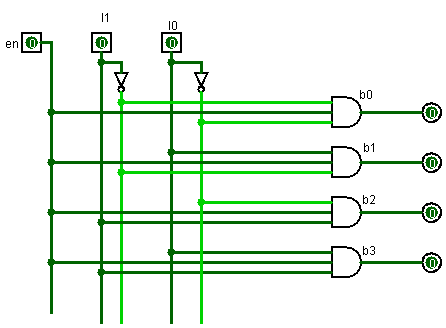
**Logic Diagram & SubCircuits:**

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**Exercise#3:** Design quad to binary (4-to-2) encoder using logic gates. Display all four input digits using seven segment displays and two output binary bits using hex displays available in logisim simulator

**Logic Diagram:**

**Exercise#4:** Design 3-to-8 decoder using two 2-to-4 decoders with enable (E) line shown in Fig. 2. Use 2:4 decoder as sub circuits in the design.

**Logic Diagram & SubCircuits:**